WHAT IS CLAIMED IS:

1. A driver circuit, comprising:

a constant current section for outputting a prescribed positive or negative current;

a first pad capable of being connected to the other end of a first resistor having its one end connected to a first node receiving a first voltage;

a second pad capable of being connected to the other end of a second resistor having its one end connected to the first node;

a first switching element connected between an output node of the constant current section and the first pad and turned ON/OFF in response to a first signal;

a second switching element connected between the output node of the constant current section and the second pad and turned ON/OFF in response to a second signal that is complementary to the first signal; and

a control section for controlling a potential at the output node of the constant current section to a prescribed potential.

2. The driver circuit according to claim 1, wherein the control section varies an on-state resistance value of the first and second switching elements according to the potential at the output node of the constant current section.

3. The driver circuit according to claim 2, wherein

the first switching element includes a first transistor connected between the output node of the constant current section and the first pad and turned ON/OFF in response to the first signal,

the second switching element includes a second transistor connected between the output node of the constant current section and the second pad and turned ON/OFF in

response to the second signal, and

the control section varies a substrate potential of the first and second transistors according to the potential at the output node of the constant current section.

4. The driver circuit according to claim 2, wherein

the first switching element includes first and second transistors connected in parallel between the output node of the constant current section and the first pad and turned ON/OFF in response to the first signal,

the second switching element includes third and fourth transistors connected in parallel between the output node of the constant current section and the second pad and turned ON/OFF in response to the second signal, and

the control section activates and inactivates the first to fourth transistors according to the potential at the output node of the constant current section.

5. The driver circuit according to claim 3, wherein the prescribed potential is set to a value close to an intermediate potential of minimum and maximum values of a gate potential of the first or second transistor minus a threshold potential of the first or second transistor.

6. The driver circuit according to claim 4, wherein the prescribed potential is set to a value close to an intermediate potential of minimum and maximum values of a gate potential of the first or second transistor minus a threshold potential of the first or second transistor.

7. The driver circuit according to claim 4, wherein

the constant current section includes a fifth transistor connected between the output node of the constant current section and a second node receiving a second voltage, and receiving a first bias at its gate,

the driver circuit further comprising:

first and second replica circuits, wherein

the first replica circuit includes a third resistor, a sixth transistor and a seventh transistor,

the third resistor is connected between the first node and the sixth transistor and has a resistance value of the first resistor scaled up at a first ratio,

the sixth transistor is connected between the third resistor and the seventh transistor, receives a second bias at its gate, and has a channel width/length ratio of the first transistor scaled down at the first ratio,

the seventh transistor is connected between the sixth transistor and the second node, receives the first bias at its gate, and has a channel width/length ratio of the fifth transistor scaled down at the first ratio,

the second replica circuit includes a fourth resistor, an eighth transistor and a ninth transistor,

the fourth resistor is connected between the first node and the eighth transistor and has a resistance value of the first resistor scaled up at a second ratio,

the eighth transistor is connected between the fourth resistor and the ninth transistor, receives a third bias at its gate, and has either a channel width/length ratio of the second transistor scaled down at the second ratio or a sum of channel width/length ratios of the first and second transistors scaled down at the second ratio,

the ninth transistor is connected between the eighth resistor and the second node, receives the first bias at its gate, and has a channel width/length ratio of the fifth transistor

scaled down at the second ratio, and

the control section activates and inactivates the first to fourth transistors based on a drain potential of the seventh transistor in the first replica circuit and a drain potential of the ninth transistor in the second replica circuit.

8. The driver circuit according to claim 7, further comprising:

a reference current circuit, wherein

the reference current circuit includes

a tenth transistor connected between the first node and the second node and receives a fourth bias at its gate, and

an eleventh transistor connected in series with the tenth transistor between the tenth transistor and the second node and receives a bias applied to the gate of the fifth transistor at its gate, and

the control section activates and inactivates the first to fourth transistors based on a comparison result between the drain potential of the seventh transistor in the first replica circuit and a drain potential of the eleventh transistor in the reference current circuit and a comparison result between the drain potential of the ninth transistor in the second replica circuit and the drain potential of the eleventh transistor in the reference current circuit.

9. The driver circuit according to claim 4, wherein a potential applied to the gates of the first to fourth transistors is lower than the first voltage.

10. A driver circuit, comprising:

a constant current section for outputting a prescribed positive or negative current;

a first pad;

a second pad;

a first switching element connected between an output node of the constant current section and the first pad and turned ON/OFF in response to a first signal;

a second switching element connected between the output node of the constant current section and the second pad and turned ON/OFF in response to a second signal complementary to the first signal;

a first resistor connected between a first node receiving a first voltage and the first pad;

a second resistor connected between the first node and the second pad; and

a control section for controlling a potential at the output node of the constant current section to a prescribed potential.

11. The driver circuit according to claim 10, wherein the control section varies an on-state resistance value of the first and second switching elements according to the potential at the output node of the constant current section.

12. The driver circuit according to claim 11, wherein

the first switching element includes a first transistor connected between the output node of the constant current section and the first pad and turned ON/OFF in response to the first signal,

the second switching element includes a second transistor connected between the output node of the constant current section and the second pad and turned ON/OFF in response to the second signal, and

the control section varies a substrate potential of the first and second transistors according to the potential at the output node of the constant current section.

13. The driver circuit according to claim 11, wherein

the first switching element includes first and second transistors connected in parallel between the output node of the constant current section and the first pad and turned ON/OFF in response to the first signal,

the second switching element includes third and fourth transistors connected in parallel between the output node of the constant current section and the second pad and turned ON/OFF in response to the second signal, and

the control section activates and inactivates the first to fourth transistors according to the potential at the output node of the constant current section.

14. The driver circuit according to claim 12, wherein the prescribed potential is set to a value close to an intermediate potential of minimum and maximum values of a gate potential of the first or second transistor minus a threshold potential of the first or second transistor.

15. The driver circuit according to claim 13, wherein the prescribed potential is set to a value close to an intermediate potential of minimum and maximum values of a gate potential of the first or second transistor minus a threshold potential of the first or second transistor.

16. The driver circuit according to claim 13, wherein

the constant current section includes a fifth transistor connected between the output node of the constant current section and a second node receiving a second voltage, and receiving a first bias at its gate,

the driver circuit further comprising:

first and second replica circuits, wherein

the first replica circuit includes a third resistor, a sixth transistor and a seventh transistor,

the third resistor is connected between the first node and the sixth transistor and has a resistance value of the first resistor scaled up at a first ratio,

the sixth transistor is connected between the third resistor and the seventh transistor, receives a second bias at its gate, and has a channel width/length ratio of the first transistor scaled down at the first ratio,

the seventh transistor is connected between the sixth transistor and the second node, receives the first bias at its gate, and has a channel width/length ratio of the fifth transistor scaled down at the first ratio,

the second replica circuit includes a fourth resistor, an eighth transistor and a ninth transistor,

the fourth resistor is connected between the first node and the eighth transistor and has a resistance value of the first resistor scaled up at a second ratio,

the eighth transistor is connected between the fourth resistor and the ninth transistor, receives a third bias at its gate, and has either a channel width/length ratio of the second transistor scaled down at the second ratio or a sum of channel width/length ratios of the first and second transistors scaled down at the second ratio,

the ninth transistor is connected between the eighth resistor and the second node, receives the first bias at its gate, and has a channel width/length ratio of the fifth transistor scaled down at the second ratio, and

the control section activates and inactivates the first to fourth transistors based on a drain potential of the seventh transistor in the first replica circuit and a drain potential of

the ninth transistor in the second replica circuit.

17. The driver circuit according to claim 16, further comprising:

a reference current circuit, wherein

the reference current circuit includes

a tenth transistor connected between the first node and the second node and receives a fourth bias at its gate, and

an eleventh transistor connected in series with the tenth transistor between the tenth transistor and the second node and receives a bias applied to the gate of the fifth transistor at its gate, and

the control section activates and inactivates the first to fourth transistors based on a comparison result between the drain potential of the seventh transistor in the first replica circuit and a drain potential of the eleventh transistor in the reference current circuit and a comparison result between the drain potential of the ninth transistor in the second replica circuit and the drain potential of the eleventh transistor in the reference current circuit.

18. The driver circuit according to claim 13, wherein a potential applied to the gates of the first to fourth transistors is lower than the first voltage.

19. A driver circuit for complementarily driving first and second output nodes in response to differential input signals, comprising:

a first driving section for driving the first output node in response to one of the differential input signals;

a second driving section for driving the second output node in response to the other differential input signal; and

a control section for controlling timing of driving the first and second driving sections so that voltage levels at the first and second output nodes switch at the same timing.